|  |
| --- |
| MICROCOM GPU v1.0 MANUAL |
|  |
| A hardware and software guide to using the Microcom GPU  10103  Authored by: J.Nock |



10103

Contents

[Technical Specifications 3](#_Toc43296579)

[Memory Map & Registers 4](#_Toc43296580)

[Memory map for EP4CE6 FPGA: 4](#_Toc43296581)

[Memory map for EP4CE10 FPGA: 5](#_Toc43296582)

[Verilog HDL notes: 5](#_Toc43296583)

[MAGGIEs 6](#_Toc43296584)

[MAGGIE Registers 7](#_Toc43296585)

[BP2RAST\_cmd 8](#_Toc43296586)

[Bits 7-6 – Text\_mode\_master / text\_mode\_slave 8](#_Toc43296587)

[Bit 4 – mode\_565 8](#_Toc43296588)

[Bit 3 – BART enable 8](#_Toc43296589)

[Bit 2 – 16\_bit\_mode 8](#_Toc43296590)

[Bits 1-0 – Video Mode / pixels per byte 8](#_Toc43296591)

[Text Mode 9](#_Toc43296592)

[DEFAULT MAGGIE SETTINGS 11](#_Toc43296593)

[PALETTES 12](#_Toc43296594)

[ARGB4444 Palette 12](#_Toc43296595)

[Host IO ports 13](#_Toc43296596)

[Appendix A – Character Codepage 14](#_Toc43296597)

|  |
| --- |
| Technical Specifications Depending on the FPGA used in the uCOM GPU card, the following features will be available in varying capacities. Listed below are *minimum specifications* based on an Intel EP4CE6 FPGA (used in development of the GPU):   * 22KB FPGA graphics RAM, plus 1 KB for palettes * 7 graphics layers * 640x480 resolution at 60 fps (VGA) * 4,096 colours   **NOTE:** *All 16-bit words in the uCOM GPU are big-endian*. |
|  |

|  |
| --- |
| Memory Map & Registers The uCOM GPU uses a vacant 512 KB slot in the host system’s memory space – see the uCOM’s manual for more information on this. This 512 KB window is filled with the GPU’s own RAM – if the GPU has less than 512 KB of RAM, accessing memory above the GPU’s upper memory limit will return FF values and be read-only (writes will be ignored). *Only the last 16 bytes of the last page of the 512KB will return anything other than FF, and this will be the BANK\_ID as per the uCOM’s memory specifications. This is a pseudo-ROM location, with a value returned from a hardwired value in the HDL of the FPGA.* Memory map for EP4CE6 FPGA:  * 0000-01FF – GPU HW registers:   + **00-07** = H&V triggers for 4 yellow test cursors   + **0C-0D** = H&V reset coordinates for all 15 MAGGIE\_Layer#s   + **10-13 + 4\*MAGGIE\_Layer#** = H&V top left edge of each MAGGIE\_Layer# window   + **60 + 10\*MAGGIE\_Layer#** = 16 byte controls for each of the 15 MAGGIE layers * 0200-11FF – Default IBM VGA 8x16 font. * 1200-5FFF – Video RAM (for text buffers / sprite data)   + **1200-1B5F** – Typical memory space for a full screen of text * 7C00-7FFF – Palettes:   + **7C00-7DFF** – primary palette (ARGB4444)   + **7E00-7FFF** – secondary palette (RGB565)   Without text you can mix 7 on-screen sprites, or 1 text layer and 5 sprites. Other than a RAM limitation, there are no other output limitations. Any mode and any resolution with any palette may all be mixed simultaneously onscreen. Memory map for EP4CE10 FPGA:  * 0000-01FF – GPU HW registers:   + **00-07** = H&V triggers for 4 yellow test cursors   + **0C-0D** = H&V reset coordinates for all 15 MAGGIE\_Layer#s   + **10-13 + 4\*MAGGIE\_Layer#** = H&V top left edge of each MAGGIE\_Layer# window   + **60 + 10\*MAGGIE\_Layer#** = 16 byte controls for each of the 15 MAGGIE layers * 0200-11FF – Default IBM VGA 8x16 font. * 1200-7BFF – Video RAM (for text buffers / sprite data)   + **1200-1B5F** – Typical memory space for a full screen of text * 7C00-7FFF – Palettes:   + **7C00-7DFF** – primary palette (ARGB4444)   + **7E00-7FFF** – secondary palette (RGB565)   Without text you can mix 10 on-screen sprites, or 1 text layer and 8 sprites. Other than a RAM limitation, there are no other output limitations. Any mode and any resolution with any palette may all be mixed simultaneously onscreen. Verilog HDL notes: NUM\_LAYERS = 2 through 15 = 2 layers through 15 layers.  PALETTE\_ADDR = Sets the base address for the 2 palettes.  Palettes occupy the last 1024 bytes of GPU RAM. If the RAM ends on 2^ADDR\_SIZE (i.e. 32768), then (2\*\*ADDR\_SIZE)-1024 can be used to set PALETTE\_ADDR, otherwise PALETTE\_ADDR must be set explicitly to the last 1KB of available GPU RAM. Obviously, this depends on the amount of RAM available in the FPGA used. |
| MAGGIEs The **M**ultiple **A**ddress **G**enerator and **G**raphic **I**nstruction **E**ngines are the workhorses of the GPU. There are 7 MAGGIEs in the smallest system, numbered 0-6.  All MAGGIEs have their HV resets set to HV\_Trigger 0C & 0D.  MAGGIE top-left window X/Y positions:   * MAGGIE0 at HV\_Trigger 0010-11 & 0012-13 * MAGGIE1 at HV\_Trigger 0014-15 & 0016-17 * MAGGIE2 at HV\_Trigger 0018-19 & 001A-1B * MAGGIE3 at HV\_Trigger 001C-1D & 001E-1F * MAGGIE4 at HV\_Trigger 0020-21 & 0022-23 * MAGGIE5 at HV\_Trigger 0024-25 & 0026-27 * MAGGIE6 at HV\_Trigger 0028-29 & 002A-2B * MAGGIE7 at HV\_Trigger 002C-2D & 002E-2F * MAGGIE8 at HV\_Trigger 0030-31 & 0032-33 * MAGGIE9 at HV\_Trigger 0034-35 & 0036-37   MAGGIE register addresses – 16 bytes for each MAGGIE:   * MAGGIE0 – 0060 * MAGGIE1 – 0070 * MAGGIE2 – 0080 * MAGGIE3 – 0090 * MAGGIE4 – 00A0 * MAGGIE5 – 00B0 * MAGGIE6 – 00C0 * MAGGIE7 – 00D0 * MAGGIE8 – 00E0 * MAGGIE9 – 00F0 |

## MAGGIE Registers

|  |  |  |
| --- | --- | --- |
| Address | Name | Function |
| Base + 00 | BP2RAST\_cmd | 8-bit composite. Video Mode setting. |
| Base + 01 | BP2RAST\_bgc | Background colour. |
| Base + 02 | BP2RAST\_fgc | Foreground colour. |
| Base + 03 | RST\_ADDR\_H | MSB bits of 24-bit base read address. |
| Base + 04 | RST\_ADDR\_M | MID bits of 24-bit base read address. |
| Base + 05 | RST\_ADDR\_L | LSB bits of 24-bit base read address. |
| Base + 06 | YINC\_ADDR\_H | MSB of 16-bit Y-line increment for read address. |
| Base + 07 | YINC\_ADDR\_L | LSB of 16-bit Y-line increment for read address. |
| Base + 08 | X\_SIZE\_H | MSB of 16-bit display width screen pixels. |
| Base + 09 | X\_SIZE\_L | LSB of 16-bit display width screen pixels. |
| Base + 0A | Y\_SIZE\_H | MSB of 16-bit display height screen lines. |
| Base + 0B | Y\_SIZE\_L | LSB of 16-bit display height screen lines. |
| Base + 0C | X\_SCALE | Two 4-bit words. Upper 4 controls x-increment every period, lower 4 is pixel period counter to define number of pixels until upper 4 bits are added to the address pointer. |
| Base + 0D | Y\_SCALE | Two 4-bit words. Upper 4 bits reserved for text tile mode y-size; lower 4 bits is line period counter to define number of lines until YINC\_ADDR is added to address pointer. |
| Base + 0E | X\_START\_SUB | 8-bit word. Defines an odd pixel start position within the period counter and x-position within a bit plane’s x-coordinate position. |
| Base + 0F | Y\_START\_SUB | 8-bit word. Defines an odd line start within the period counter and y-coordinates inside a font. |

### BP2RAST\_cmd

The BP2RAST\_cmd register is composed of the following bit settings:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| text\_mode\_master | text\_mode\_slave | not used | mode\_565 | bart\_enable | 16\_bit\_mode | Video Mode | Video Mode |

### Bits 7-6 – Text\_mode\_master / text\_mode\_slave

When using text/font/tile mode, two adjacent MAGGIEs must be used. The first one must have the '*text\_mode\_master*' bit set in the '*BP2RAST\_cmd*' while the second MAGGIE must have the '*text\_mode\_slave*' bit set in the '*BP2RAST\_cmd*'. These bits must be zero for graphics output.

### Bit 4 – mode\_565

### Bit 3 – BART enable

This bit must be HIGH for the linked BART to output pixel data. If the bit is LOW, the MAGGIE/BART pipeline is effectively turned off, unless the MAGGIE is a text\_mode\_master.

### Bit 2 – 16\_bit\_mode

If HIGH, the BART works in 16-bit mode (so all addresses must be even) to use two-byte words when reading the pixel data.

### Bits 1-0 – Video Mode / pixels per byte

Determines the Video Mode, or pixels per byte. The table below shows how bits 2-0 work together to determine the Video Mode:

|  |  |  |  |
| --- | --- | --- | --- |
| Bit 2 | Bit 1 | Bit 0 | Video Mode |
| 0 | 0 | 0 | 1-bit colour |
| 0 | 0 | 1 | 2-bit colour |
| 0 | 1 | 0 | 4-bit colour |
| 0 | 1 | 1 | 8-bit colour |
| 1 | 0 | 0 | 16-bit, 8 pixels-per-word |
| 1 | 0 | 1 | 16-bit, 4 pixels-per-word |
| 1 | 1 | 0 | 16-bit, 2 pixels-per-word |
| 1 | 1 | 1 | 16-bit, true colour |

## Text Mode

Two MAGGIEs are required for text mode – a master and a slave – and they must be adjacent to each other (i.e. MAGGIE0 & MAGGIE1, MAGGIE3 & MAGGIE4 etc).

The master MAGGIE is responsible for the positioning of the window on the screen and pointing to the source data (*screen buffer*), whereas the slave MAGGIE controls the foreground and background colours.

The screen buffer location is specified in the master MAGGIE in the 24-bit word at register addresses +3 to +5.

The Video Mode in both MAGGIEs must match, except in the master where the BP2RAST\_cmd BART\_enable (bit 3) must be disabled; otherwise you will get junk on the screen.

In 16-bit text mode, each character tile is followed by a palette byte. The upper 4-bits control the foreground colour, the lower 4-bits control the background colour.

All other controls are the same as when using it as a bitmap graphics window.

The '*font\_y\_size*', combined upper bits of '{hw\_regs[Y\_START\_SUB][7:6], hw\_regs[Y\_SCALE][7:4]}' in the *text\_mode\_master* which must also be set to the font/tile height -1 (e.g.: 0=1 line, 7=8 lines, 15=16 lines, 31=32 lines) when in text/font/tile master mode.

For the *'text\_mode\_slave*' MAGGIE, the only functioning 4 controls are:

1. reset\_addr which points to the base memory address for font/tile graphics data,
2. period\_x[4] which defines a font as 16 pixels wide when set, or 8 pixels when low, and period\_x[3:0] which mask out the upper bits for fonts/tile addressing for 256, 512, 1024, 2048, 4096 characters (used in 16 bit addressing mode, otherwise set these bits to 0),
3. period\_y[1:0] which defines the font height (0=8, 1=16, 2=32, 3=64 lines tall), and
4. BP2RAST\_cmd which should match the *text\_mode\_master* MAGGIE settings except for the master and slave bit.

All base memory address settings should be on an even byte when using 16-bit mode. Fonts/tile graphics data should always begin on an even byte address.

## DEFAULT MAGGIE SETTINGS

Example default MAGGIE settings for the ‘chip’ image:

Top image: MAGGIE4 - HW triggers @ 20-21 & 22-23

A0 - 1A 10 00 00 33 00 00 60 00 BF 00 77 00 00 00 00

Middle image: MAGGIE5 - HW triggers @ 24-25 & 26-27

B0 - 1A 70 00 00 33 00 00 60 00 BF 00 77 01 01 00 00

Background image: MAGGIE6 - HW triggers @ 28-29 & 2A-2B

C0 - 0A B0 00 00 33 0A 00 60 00 BF 00 77 03 03 00 00

# PALETTES

The palettes are held in memory at $7C00-$7FFF and are 512 entries wide, with the 4444 colour palette occupying the first 256x16 entries while the 565 palette occupies the second 256x16 entries. Both palettes are 16-bit.

## ARGB4444 Palette

This is the default palette for Text Mode, requiring two bytes per palette entry. As it is commonly used with Text Mode, which can specify a maximum of 16 index values, it is generally divided into separate palettes of 16 entries, with the first 16 being the default palette.

Each entry consists of two bytes, as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| 1st BYTE | | 2nd BYTE | |
| 4-bits | 4-bits | 4-bits | 4-bits |
| Transparency | RED | GREEN | BLUE |

The last four pages of Bank 0x41 contains the palette, with the first 32 bytes containing the default palette.

# Host IO ports

The GPU exposes some specific IO addresses to the host to facilitate extra hardware functions, listed below. The IO addresses are separate from the GPU RAM address space and are easily customizable in Quartus via the parameter settings in the Z80\_bridge.

|  |  |  |
| --- | --- | --- |
| **IO Address** | **Read/Write** | **Function** |
| **240 / F0** | Read-only | PS2 data (keyboard interface) |
| **241 / F1** | Read-only | PS2 status (~0=data ready) |
| **242 / F2** | Write-only | Speaker/sound enable (0=off, ~0=on) |
| **243 / F3** | Write-only | Video output enable (0=off, ~0=on) |

## Appendix A – Character Codepage

